test circuits with an IC chip since the method improves circuit density per area by limiting the formation of the two elements in separate wafers.

Applicant has carefully considered the two new cited prior art references in the Examiner's grounds of rejection, and respectfully submits that new claims 9 through 12 recite patentable subject matter.

New independent claim 9 recites a semi-conductor chip package which includes the following features:

"a lead frame including a frame body, at least two chip-receiving windows formed in said frame body... and a plurality of external connection leads formed on said frame body adjacent to at least one of said chip-receiving windows...

... a master integrated circuit chip, and ... a slave integrated circuit chip, wherein said master integrated circuit chip includes an embedded testing circuit to permit testing of said slave integrated circuit chip . . .; and

wherein said external connection leads are electrically connected to said bonding pads other than to bonding pads on said slave integrated circuit, said external connection leads serving as terminal pins such that external electrical connection with said integrated circuit chip in said at least one of said chip-receiving windows is established via said external connection leads."

Although the Examiner states that Yukio may not have classified the IC chips as master and slave IC's, there is nothing in the Yukio document that would teach one away from that concept by eliminating the application and the structure to specify integrated circuits.

Neither Yukio nor Taniguchi et al. teach the limitations of claim 9 that "said external connection leads are electrically connected to said bonding pads on said integrated chip in said at least one of said chip-receiving windows other than said slave-integrated circuit." As the Examiner acknowledges, Yukio does not disclose an embedded testing circuit.

While Taniguchi et al. does demonstrate a test circuit for an embedded memory, the test circuit namely, the DRAM 1, is directly connected to the external pins 3. In the Taniguchi et al. test circuit and test method, there is no disclosure of the test circuit with memory being connected by only internal leads to a slave IC chip, all contained within a semiconductor chip package. Referring to the Abstract and the drawings of the Yukio reference, it is also clear that both chips 11 and 12 are directly electrically connected to external leads 13. The cited new prior art references would not lead one having ordinary skill in the art to the claimed subject matter since in the case of Yukio, each integrated circuit is connected to external leads, and in the case of Taniguichi et al., the slave integrated circuit is still connected to external leads. In view of these differences, Applicant respectfully submits that new claim 9 patentably distinguishes over the newly cited prior art and respectfully requests allowance of same.

With respect to new claim 12, which depends on claim 9, neither Yukio nor Taniguchi et al. discloses or suggests the testing process of the semi-conductor chip package, wherein said "master integrated chip is configured to receive stimulating signals via said external connection leads to stimulate said slave integrated circuit chip via said internal connection leads in response to the stimulating signals to receive stimulation response of said slave integrated circuit via said internal connection leads, and to output information corresponding to the stimulation response via said external connection leads."

Accordingly, Applicant respectfully submits that claims 9-12 recite novel and unobvious inventive matter and should be allowed. If the Examiner has any questions, a telephone call to the undersigned will be appreciated.

Respectfully submitted,

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